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Mitigating the Impact of NBTI and PBTI Degradation

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Abstract

Modern CMOS devices encounter a major problem that alters the threshold voltages of the NMOS and PMOS. Negative Bias Temperature Instability (NBTI) and Positive Bias Temperature Instability (PBTI) are common ageing phenomena observed in PMOS and NMOS devices, respectively. Due to operating temperature and stress time, NBTI and PBTI create a decrease in drain-to-source current and an increase in propagation delay. Threshold voltage is an important parameter due to exponential dependence on delay and leakage power. Threshold voltage variations produce adverse effects on operation frequency. These phenomena accrue in pull-up/pull-down transistors in stack and vastly degrade CMOS performance. This paper discusses the various factors responsible for NBTI and PBTI and the challenges associated with modeling these effects due to the recovery mechanism exhibited by the transistors when the stress is removed. Therefore, we propose an algorithm to reduce the effects of NBTI and PBTI that will reduce the stress time for each transistor through the relative repositioning of the transistors based on the signal probability.

Keywords: Negative Bias Temperature Instability (NBTI); Positive Bias Temperature Instability (PBTI); Operating voltage; Temperature

Introduction

Negative Bias Temperature Instability (NBTI) and Positive Bias Temperature Instability (PBTI) [1,2] are caused by a combination of elevated temperatures and negative/positive gate voltages respectively [3,4]. This results in an increase/decrease in the threshold voltage and can deteriorate the performance of CMOS circuits. Variation in threshold voltage will have adverse effects on current and propagation delay and in turn on frequency of operation. This phenomenon can accrue for both pull-up and pull-down transistors in stack, degrading the device performance. This paper provides for a solution that implements an algorithm to reduce the effects brought on by the NBTI and PBTI phenomena.

Threshold voltage shifts can be caused by variations in fixed charge density and interface-trapped charge density. Interface traps (referred to as permanent traps due to their extremely slow recovery time) are interfacing trivalent Si atoms with an unsaturated valence electron at the SiO_2-Si interface [4]. These interfaces attract holes that weaken the Si-H bonds until the bonds break. The H released diffuses into the Si, leaving behind an interface trap resulting in V_{th} degradation. In scaled devices at technology nodes of 45 nm and below, high k materials are used to reduce leakage and improve the I_{ON}/I_{OFF} ratio. In these materials, PBTI creates bulk traps in NMOS, comparable to NBTI in PMOS at 45 nm and below. In PMOS devices, an increase in V_{th} results in a decrease in V_g-V_{th} which reduces current and results in frequency degradation of ring oscillators [5,6]. Stress can be dynamic or static. Dynamic stress is caused by the toggling of signals between 0 and 1, deteriorating the device at a slow and non-deterministic rate. NBTI and PBTI would be most dominant for signals subjected to a static stress which is terminated when degradation is relaxed and when the stress is removed for sufficiently long time. Some devices may be subject to either static or dynamic stress leading to asymmetric degradation in timing paths which in turn results in setup time failure.

Past solutions to mitigate the impact of NBTI and PBTI include the development of NBTI/PBTI-aware processing steps for CMOS devices via the use or removal of hydrogen [7], nitrogen [8], fluorine [4], and water during oxide growth [4]. Others involve modifications of the circuit such as the investigation of the input vector control technique [9], logic restructuring and pin reordering along timing critical paths through the detection of functional symmetries, transistor stacking [10], and transistor arrangement restructuring in the PMOS pull-up plane [3]. Unfortunately, the above solutions are only specific to a particular design and are more focused towards modifying the processing steps. To avoid this result, there is a need to address the problem and take into account the probable use cases for a given chip.

In this paper, we discuss various factors responsible for NBTI and PBTI and the challenges associated with modelling this effect due to the recovery mechanism exhibited by the transistors when stress is removed. We also propose an algorithm to restructure the CMOS device that can help mitigate the impact of NBTI and PBTI when the device is operating in field. This serves as an extension to a previously proposed restructuring algorithm [3], which takes into account arbitrary signal probabilities at the inputs of the individual transistors.

The rest of the paper is organized as follows: In section 2, we explain various factors affecting NBTI and PBTI, the origin of these phenomena, and the detrimental impact they have on transistor performance. In section 3, we discuss the proposed algorithm and the methodology to reduce the impact of NBTI and PBTI. Results and analysis are outlined in section 4. Finally, conclusions and future research are drawn in section 5. A preliminary short version of this paper appears in the 2nd World Congress on Automation and Robotics [1].

Factors Affecting NBTI and PBTI

In this section, we will discuss the impact of various factors that affect the device performance due to NBTI and PBTI. The factors that

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primarily contribute to NBTI and PBTI are the operating voltage, temperature, and stress time.

Operating voltage

As the operating voltage increases, the negative bias of the PMOS transistors increases, which in turn increases the NBTI degradation. Scaling of technology node leads to high electric fields at the gate, causing NBTI. Higher operating voltages result in higher electric fields across the device junction resulting in higher stress.

Temperature

The effect of NBTI worsens at an elevated temperature and shows exponential dependence due to the increasing dissociation of Si-H bonds at high temperature. Typical stress temperatures range from 100°C to 250°C, encountered during burn-in [4]. During extremely high performance applications, possibly at the highest operating frequencies, the higher toggling activity of signal nets can result in formation of local hot-spots inside the chip's functioning major parts, resulting in an elevated temperature in some parts of the chips.

Stress time

Signal probability, the probability of input voltage to turn on gate of PMOS/NMOS, governs the total time during which a transistor experiences stress. The probability of signal at a PMOS/NMOS gate being 0/1 will govern the NBTI/PBTI impact respectively. For transistors connected in stack, degradation due to NBTI and PBTI cannot be considered individually because it becomes a function of signal probabilities of transistors present up and down in the stack for PMOS and NMOS, respectively.

When there are many transistors connected in series, the equivalent signal probability is taken into consideration for stress time. The proposed algorithm assists in deciding which CMOS structure would have the least amount of stress time, which holds the minimal NBTI/PBTI effect. While reordering the PMOS/NMOS transistors for observing the NBTI/PBTI effect, the fact that the PMOS and NMOS transistors connected to the power supply and ground, respectively, suffer more degradation than the transistors not directly connected along with the signal probability must be taken into consideration to ensure that the logic structure is more robust to the NBTI/PBTI effect.

The variation in the threshold voltage is caused by variations in fixed charge and interface trapped charge density, also referred to as permanent traps. Due to the unsaturated valence electron at the SiO_2-Si interface, holes are attracted, weakening the Si-H bond, resulting in V_{th} degradation. Due to technology scaling down and the use of high k material, the PBTI creates a bulk trap similar to an interface trap of SiO_2 in NBTI. The stress is categorized as dynamic and static stress. In any system, there could be some devices which are under static and dynamic stress where the NBTI and PBTI effects, respectively, are dominant, leading to an asymmetric degradation in the timing paths and resulting in the functionality failure of the device. Various methods in processing and restructuring of the transistors are implemented to mitigate the NBTI and PBTI effects.

Algorithm

The proposed algorithm assists with deciding the CMOS structure in which there is minimum probability of the device being under stress. The algorithm's process is based on the fact that PMOS and NMOS transistors connected to the power supply and ground, respectively, suffer more V_{th} degradation than the ones not directly connected to it [3]. Therefore, in order to mitigate NBTI, the algorithm reorganizes the circuit structure by taking into account the relative positions of transistors and the number of the PMOS networks directly connected to VDD in the stack. This is valid while assuming equal signal probabilities for all the inputs. However, this is not a practical assumption. As explained in the previous section, when two or more transistors are connected in a stack, the probability that a given transistor is under stress is a function of the signal probabilities of the other transistors in the stack. Therefore, apart from the number and the relative position of the transistors, the signal probabilities must be taken into account when deciding which logic structure would be most robust to the impact of NBTI or PBTI.

In this proposed algorithm, the "probability of degradation" for each PMOS and NMOS input, respectively, is calculated by multiplying the signal probability at its input by the worst case signal probability of the PMOS transistor stacked above it or by the worst case signal probability of the NMOS transistor stacked below it. The probability of degradation (PD) and signal probability (SP) are related by the following expression:

PMOS: PDi, NBTI = SPi . $\prod$ (SP) stacked above

and

NMOS: PDi, PBTI = SPi . $\prod$ (SP) stacked below

If there are any parallel transistors in stack above, the highest signal probability is taken into account causing maximum degradation due to NBTI or PBTI. To illustrate the probability of degradation and total switching activity parameters, two different implementations for the AOI gate are taken into consideration. Depending on the signal probabilities, the probability of degradation is calculated at each input for a given circuit. The total switching activity or equivalent stress time is calculated as the sum of the probability of degradation at each input. The structure with the smallest total switching activity will undergo the least amount of NBTI or PBTI degradation. The structure with smallest total switching activity is preferred in order to reduce the aging caused by the stress time factor which enhances the effect of NBTI.

Results and Analysis

Consider (Figure 1) which shows two implementations of an AOI gate using CMOS transistors. Assuming equal signal probabilities, the structure (b) is more resilient to the effect of NBTI because the signal a shields the PMOS transistors with signals b and c. The effective signal probability at b would be the multiplication of signal probability at and the signal probability at b. The same argument holds true for the PMOS transistor c. Therefore, the effective probabilities for structure b are as shown in (Table 1).

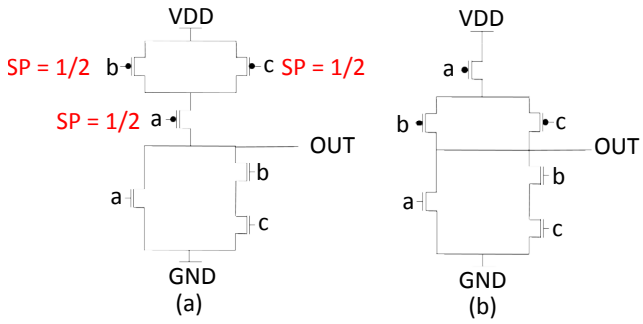

Figure 1: Two implementations of an AOI gate using CMOS transistors.

Signal	Structure (a)	Structure (b)
a	(½) x (½)=(¼)	(½)
b	(½)	(½) x (½)=(¼)
c	(½)	(½) x (½)=(¼)
Total	(½) + (½) + (¼)=1.25	(¼) + (¼) +(½)=1

Table 1: Probability of degradation for the two structures with equal signal probability.

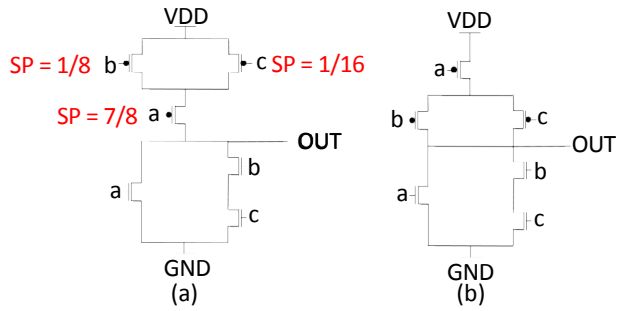

Figure 2: Unequal signal probabilities at the inputs.

Signal	Structure (a)	Structure (b)
a	(7/8) x 1/8)=(7/64)	(7/8)
b	(1/8)	(1/8) x (7/8)=(7/64)
c	(1/16)	(7/8) x (1/16)=(7/128)
Total	19/64=0.296	133/128=1.039

Table 2: Probability of degradation for the two structures with unequal signal probability.

Total switching activity or the equivalent stress time for structure (b) is 1, while for structure (a) is 1.25. Therefore, it can be concluded that structure (b) would be subjected to less stress over the lifetime of the chip as compared to structure (a) and, therefore, is more resilient to NBTI.

Now, let us consider unequal signal probabilities at the inputs as shown in (Figure 2). As evident from Table 2, the total switching activity or the equivalent stress time for structure (a) is 0.296, while for structure (b) is 1.039. Therefore structure (a) is subjected to around 3.5 times less stress than structure (b) and is better (Table 2).

These two examples show that it is possible to similarly compute the total switching activity, or the equivalent stress time considering the signal probabilities corresponding to the most common use cases and decide the structure of the CMOS devices accordingly.

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Conclusion and Future Research

In this paper, we build on an existing algorithm to design a solution which will mitigate the impact of NBTI and PBTI within any device in operation. By calculating the CMOS signal probabilities, devices can be analyzed and narrowed down to more preferable structure configurations. The structure with the smallest total switching activity is preferred in order to reduce the aging caused by the stress time factor which enhances the effect of NBTI; thus, the CMOS structure with the lowest probability of being stressed can be determined. The structure would be subjected to less stress over the lifetime of the chip than it would without the application of the proposed algorithm, making it more resilient to NBTI. This translates into a low probability of aging-related chip failure, which greatly enhances the chip reliability and allows for the reduction of CMOS degradation over time. This concept ensures that CMOS structures are created to perform its functions at the optimal level for a longer period of time.

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